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Photonic Crystal based ultra-thin "TM-only" all-optical logic gates

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Abstract

In this study, the authors propose a novel design for all-optical logic gates based on the interference effect methodology of constructing two-dimensional "photonic crystals". The gates consist of ellipse-shaped rods with a 45˚ orientation arranged in a square lattice. These rods are air-filled holes drilled in a Silicon substrate. The suggested structure is engineered to operate with Transverse Magnetic (TM) waves, which are defined such that the Transverse Magnetic polarization of light is parallel to the rods of the design while propagating. Numerical simulations demonstrate that the gates successfully meet their targeted truth tables at the communication wavelength of 1550 nm (the commonly used wavelength in optical communication). The design has ultra-small device dimensions of 4x4 μm^2, which provides the advantage of high device speed (60~110 fs). Furthermore, our design operates with TM waves, which are challenging to manipulate.

Keywords: Photonic crystals – 'All-Optical' logic gates– TM–ultra-small devices

1. Introduction

The utilization of light manipulation has emerged as the next generation of electronics, following the declining revolution of transistors [1]. In order to accelerate data processing, photons have replaced electrons as the primary means of data transfer, leading to the rise of all-optical data processing. Consequently, researchers have been motivated to develop all-optical networks, components, waveguides, adders, processors, and other related technologies to meet the demands of this new era of data processing. Photonic crystals (PHCs) have been the center of focus since their initial introduction in 1987 [2], due to their potential to create faster, smaller, and less complex computing devices. All-optical logic gates are crucial components of the future all-optical computers assembled by PHCs, leading to a significant interest in this field.

Various techniques have been adopted to manipulate light, such as (Self-collimated beam [3] , Multi-Mode Interference [4], interference based gates[5] , Mach Zehnder Interferometer[6] , and nonlinear effects of materials.

Interference effect methodology has been considered the simplest and least time-consuming method, with ease of fabrication [7],[8]. The methodology involves creating waveguides [9], [10]through the adopted main structure. Hence, enabling light to travel through, causing a constructive (logic 1) or destructive (logic 0) interference between light beams, producing the all-optical logic gate output down another waveguide. Although several researchers have made significant progress in this area, handful have figured out how to manipulate light in the TM mode.

While TE-only polarization has been widely achieved, achieving polarization-free operation is challenging due to the need to use nonlinear effects in materials, as previously defined in [11][12], hence increasing the complexity. In contrast, TE-only polarization has been introduced in many researches as [13]–[17] as it is easily manipulated through waveguides. Square or triangular lattice can be used depending on the structure and its output. Also other utilized techniques, such as ring resonators[18][19]. Cascaded all-optical logic gates were also used to posit more gates as in [20]-[21]. TM polarization was not introduced so far alone in any research, but as aforementioned, it was introduced with TE polarization, but in more complex designs.

Shapes of rods in conjunction with those of the lattice play a huge rule in determining the band width and size [22]. Here, we use oriented oval rods with square lattice to maintain the gap needed as was found in [23] The self-assembled system exhibits a TM band gap that can exceed the TM band gap of its perfect system counterpart, characterized by rods.

In this paper, we introduce TM-only polarization with a very-small-dimension design which has the privilege of easier manufacturing and implementation and is suitable for all-optical future computers. In addition, all the gates are acquired with the same design. This paper is organized as; section two introduces the new gates design and their functionality, section three displays our numerical results, in section four we discuss the time response for each output of our gates and section five exhibits the final conclusion and the future work based on this proposed structure.

2. Design and structure

Herein is a new unique design for four all-optical (PHCs based) logic gates with dimensions of 4×4 µm with (11) columns and (11) rows working with TM polarization of light (TM mode is defined such that the Transverse Magnetic polarization of light is parallel to the rods of the design while propagating). The lattice constant of this design is set to 0.38 µm containing air-drilled holes in Si substrate with refractive index of 3.45 and aligned in a square lattice as shown in Figure1. The air-holes are 45˚-oriented ellipse shaped with major and minor radii of 0.289a and 0.42a respectively. This design has a bandgap in the range between (1.468~1.645) µm of wavelength as shown in Figure 2 . The mid of this gap is λ=1.55 µm as shown in table 1. This is the wavelength we are operating within this research and also is the most common bandwidth in telecommunications.

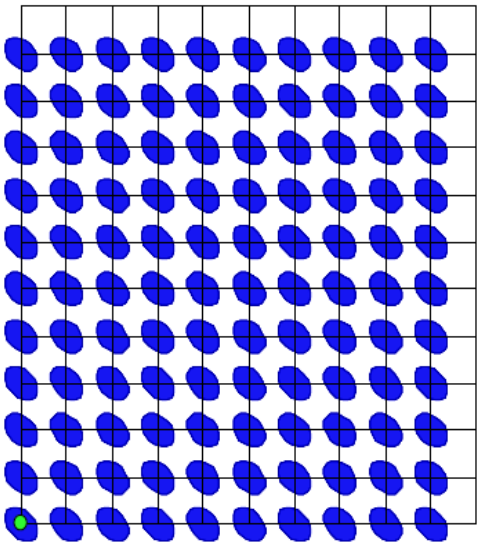

Figure 1 (the main structure: 45˚ oriented-ellipse-air-rods in Si substrate)

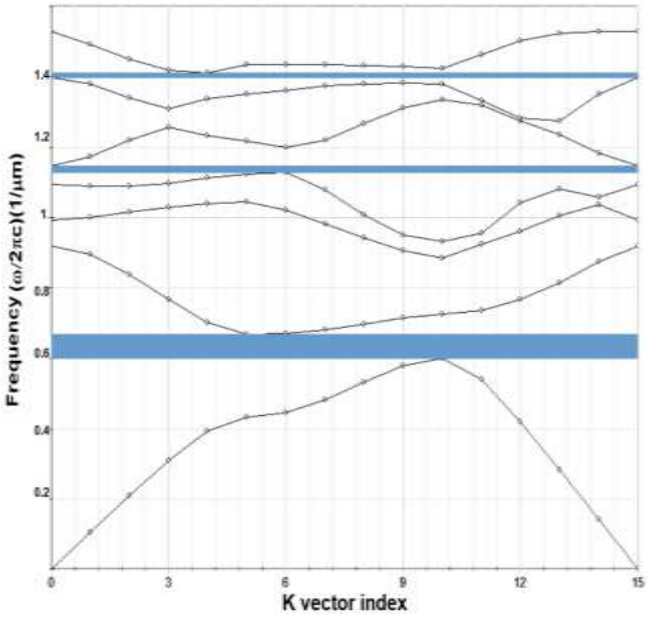

Figure 2 : (TM band gap for oriented-ellipse-air-rods in Si substrate design)

Table 1 : structure and simulation parameters

Parameters of the structure	
Dimensions of the structure	4 µm × 4µm
Refractive index of Si	3.45
minor radius of air holes	0.11 µm
major radius of air holes	0.16 µm
Lattice constant	0.38 µm
operating wavelength	1.55 µm
Optimizing rounded air-rod	0.1 µm
Tilting angel	45˚
Simulation parameters	
Boundaries of our structure	PMLs
Input wave	Continuous wave
Input power (P_{in})	10 W

Our design is composed of three input "waveguide" ports and one output "waveguide" port, the three input ports are the waveguides entitled "A, B and Ref" respectively. The output port is the waveguide we receive output through and entitled "C" as shown in Figure 3. The input and output waveguides were made by removing rods from the Si substrate so the light can travel through the air-filled them. Also, there is an optimizing air-rod added to enhance the gate inputs and outputs has minor and major radii of (0.263a,0.368a) respectively and a rotating angel of 45°. As we mentioned before all the gates are working with TM polarization. The output is considered to be logic "0" if it is 0.45 or lower of the input power and logic "1" if it is 0.55 or higher of the input power.

This work was executed using the free software of Finite-Difference Time-Domain "OptiFDTD" from Optiwave Systems Inc [24] [25] . This structure's boundaries were adjusted to (PMLs) Perfectly Matched Layers. Evaluating our gates' performances, we used the contrast ratio (CR), circumscribed as the fraction of the output powers of logic "1" and logic "0" as comes next:

$$CR = 10 \log \frac{P_1}{P_0}$$

As P1 refers to the power of output logic "1"and P0 is the output power of logic "0", Pin is the input power to all inputs A, B and Ref and it simultaneously spreads through them.

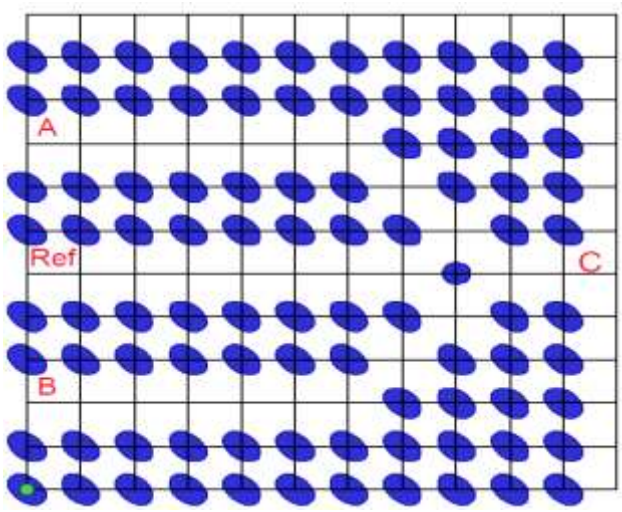

Figure 3 (all-gates structure: A and B are the main gate inputs; Ref is the controlling signal and C is the output)

3. Simulation and Numerical results

Those gates were designed to focus on TM polarization, ease of fabrication and compact dimensions and moreover higher speed. The basic theory as per optics' science of those gates' mechanism is the interference effect. So, if the three inputs are in phase (means the phase difference is 0) so a constructive interference arises and a logic "1" is created at the output, otherwise the inputs are out of phase (one or more are with phase difference π or its multiple) a destructive interference occurs revealing a logic "0" at the output. The input power was set to be Pin =10 watt of continuous wave (CW) and the reference gate is the controller of the other two gates.

I. AND all-optical logic gate:

This AND gate was established with the aforementioned design to accomplish the truth table of a normal logic AND gate as in table "1". So, if at least one of the inputs is recognized as logic "0", the output should be logic "0"as shown in Figure4(a, b). Only if

the two inputs are logic “1” that grant an output equal to logic “1” as in Figure4(c).

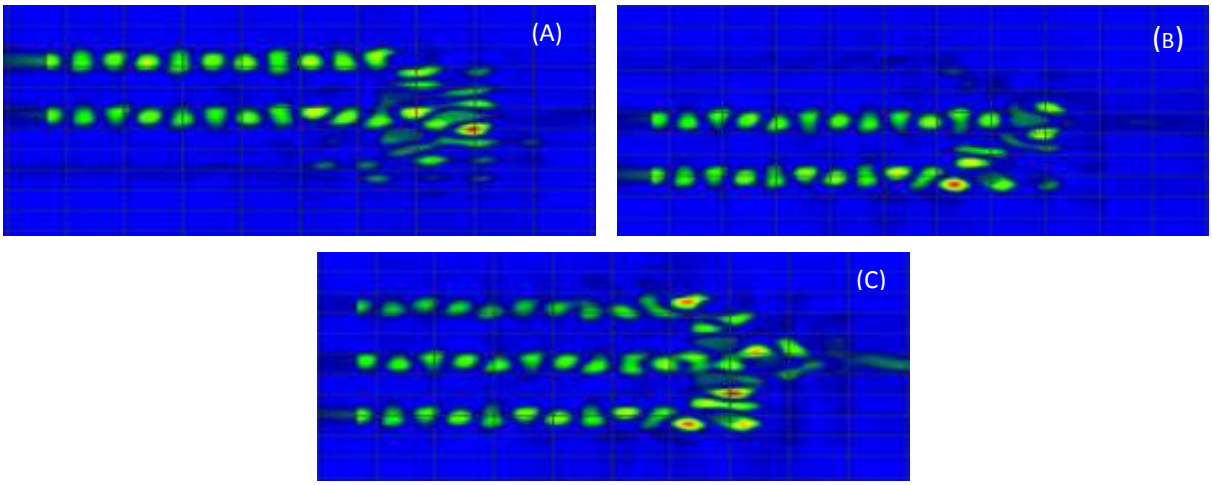

Figure 4 : input A matches logic “zero”, input B matches logic “one”, Ref is out of phase with A&B and the output matches logic “zero”, (b): input A matches logic “one”, input B matches logic “zero”, Ref is in phase with A&B and the output matches logic “zero”, (c): input A matches logic “one”, input B matches logic “one”, Ref is in phase with A&B and the output matches logic “one”)

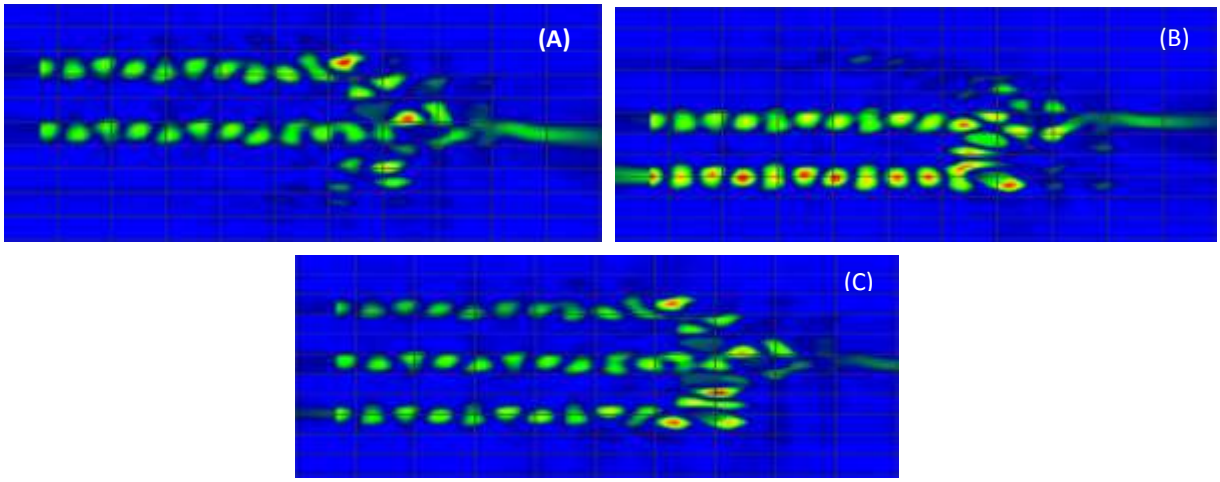

Figure 5 ((a): input A matches logic “zero”, input B matches logic “one”, Ref is out of phase with A&B and the output matches logic “one”, (b): input A matches logic “one”, input B matches logic “zero”, Ref is in phase with A&B and the output matches logic “one”, (c): input A matches logic “one”, input B matches logic “one”, Ref is in phase with A&B and the output matches logic “one”)

The AND all-optical logic gate truth table:

Table 2(AND gate: both logic and optic truth table)

AND	A	B	Ref	C	Optical Power output
	0	1	0 φ(0)	0	0.43 P_0
	1	0	1 φ(π)	0	0.23 P_0
	1	1	1 φ(0)	1	1.02 P_0

Where, P0 is defined as the input power of A and B and the contrast ratio of this gate is 6.47 computed as the percentage of the highest output logic "1" to the lowest output logic"0".

II. OR all-optical logic gate:

Using the all-gates shape previously shown, also an OR gate is accomplished satisfying the OR logic gates truth table so that: if at least one of the inputs is recognized as logic "1", the output is considered logic "1" as shown in **Error! Reference source not found.**

The OR all-optical logic gate truth table:

Table3 (OR gate: both logic and optic truth table)

OR	A	B	Ref	C	Optical Power output
	1	0	1 φ(0)	1	1.26 P_0
	0	1	1 φ(π)	1	0.8 P_0
	1	1	1 φ(0)	1	1.02 P_0

III. NOT and XNOR all-optical logic gates:

In the NOT logic gate, when both inputs are logic "0" the output is a correspondent logic "1", as Shown in Figure 6, the constant ratio of Not gate is 2.6. The following cases of XNOR gate is the same as (a), (b) and (c) in Figure 4 which is satisfied with our all-optical logic gate as illustrated below.

The NOT all-optical logic gate truth table:

Table 4 (NOT gate: both logic and optic truth able)

NOT	A	Ref	C	Optical Power output
	0	1 φ (0, π)	1	0.58 P_0
	1	1 φ(π)	0	0.32 P_0

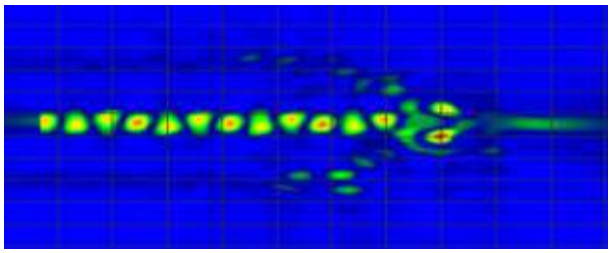

Figure 6 (input A matches logic "zero", input B matches logic "zero", the output matches logic "one")

The XNOR all-optical logic gate truth table:

Table 5 **(XNOR gate: both logic and optic truth table)**

XNOR	A	B	Ref	C	Optical Power output
	0	0	1 φ(0,π)	1	0.58 P_0
	0	1	1 φ(0)	0	0.43 P_0
	1	0	1 φ(π)	0	0.23 P_0
	1	1	1 φ(0)	1	1.02 P_0

The contrast ratio of XNOR gate is 6.47.

IV. NAND and NOR all-optical logic gates:

Both NAND and NOR gates split up some of their output with both AND and OR gates. As NAND gate shares the first two cases (A) and (B) of OR gates as in figure (5). NOR gate share the first two cases of AND gate as in figure (4). The unique case for both NAND and NOR gates is when both inputs are logic "1" and the output is logic "0" as shown in figure (7). The output for the first case of NAND and NOR gates is assigned in NOT gate figure (5). The contrast ratio for NAND gate is 6 and for NOR gate is 4.

The NAND all-optical logic gate truth table:

Table 6(NAND gate: both truth table and optic truth table)

NAND	A	B	Ref	C	Optical Power output
	0	0	1 φ(0,π)	1	0.58 P_0
	1	0	1 φ(0)	1	1.26 P_0
	0	1	1 φ(π)	1	0.8 P_0
	1	1	1 φ(π)	0	0.32 P_0

The NOR all-optical logic gate truth table:

Table 7(NOR gate: both truth table and optic truth table)

NOR	A	B	Ref	C	Optical Power output
	0	0	1 φ(0,π)	1	0.58 P_0
	1	0	1 φ (π)	0	0.23 P_0
	0	1	1 φ (0)	0	0.43 P_0
	1	1	1 φ (π)	0	0.32 P_0

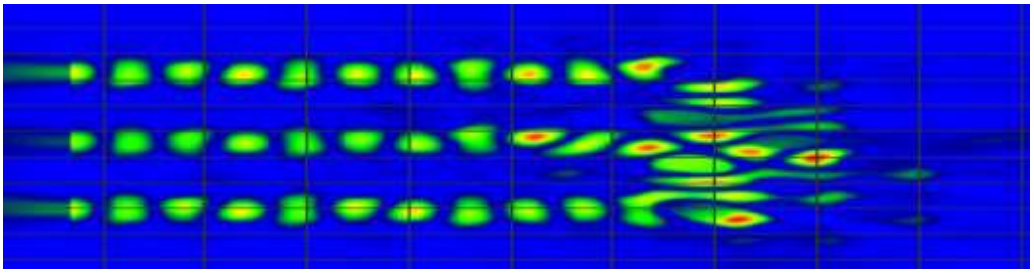

Figure 7 (input A matches logic" one", input B matches logic" one" and the output is logic "zero".

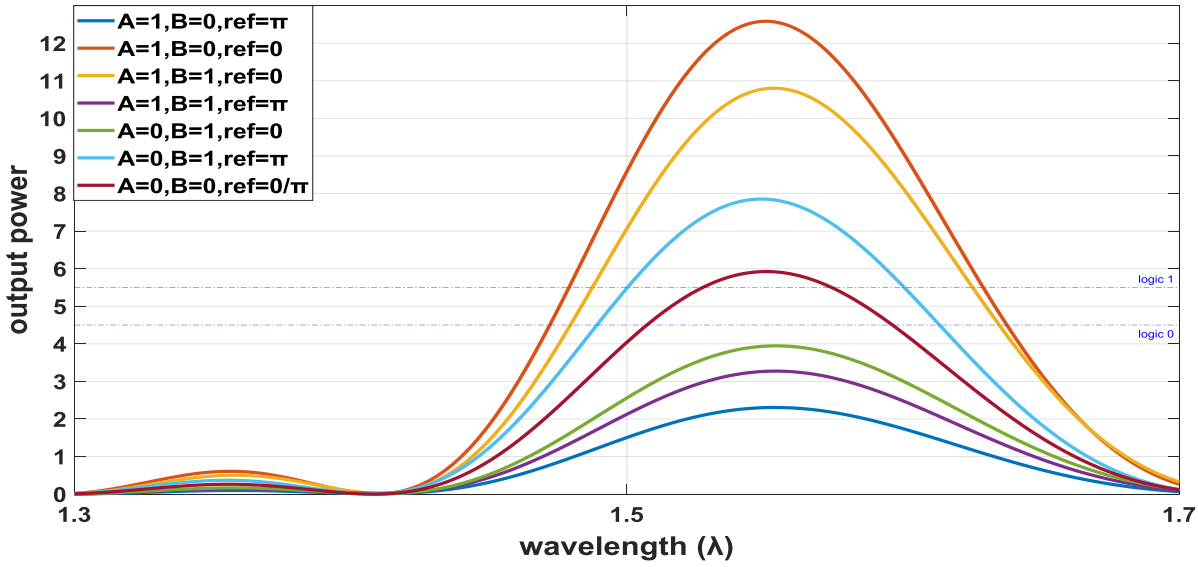

Figure 8 the output power for all input cases, separating 7 cases between four on (logic “one”) and three off (logic “zero”)

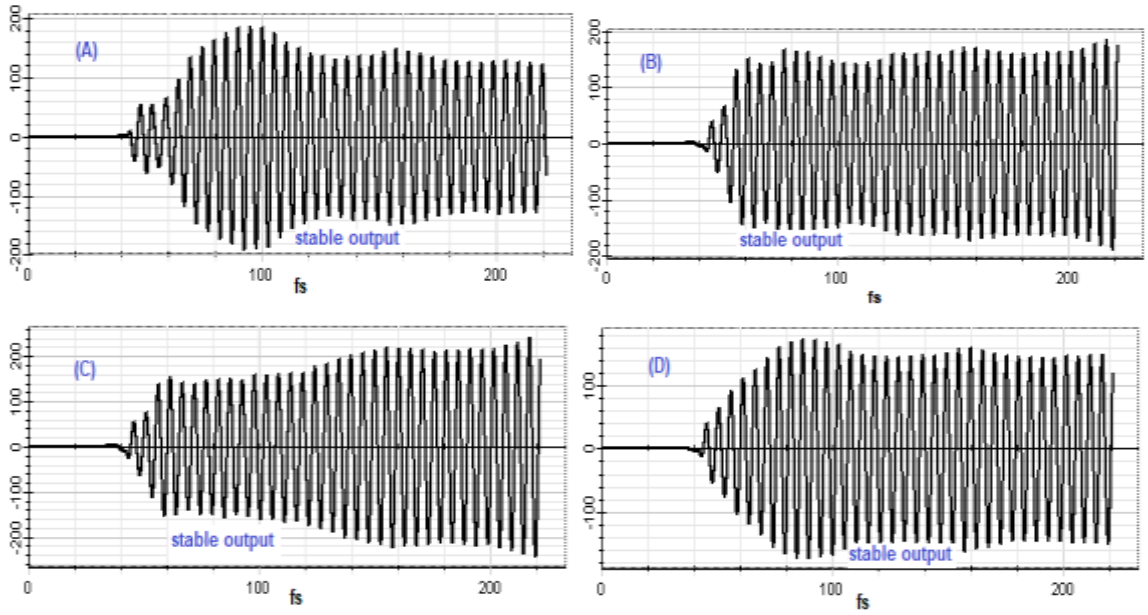

Figure 9 (output latency four cases:(A) A=1, B=0, Ref is out of phase and C=0 with latency 110 fs, (B) A=1, B=0, Ref is in phase and C=1 with latency 60 fs, (C) A=1, B=1, Ref is in phase and C=1 with latency 60 fs, (D) A=0, B=0, Ref is indifferent and C=1 with latency 100 fs)

4. Power output and Time response for all gates:

In this section we particularly discuss the power output for all cases and the latency of our all-optical logic gates, the results were found optimistically odd. The power output for all cases were divided into two sections separated by margin of neither logic one or logic zero between output power (4.5,5.5) shown in figure 8. On the other hand, the best time response of the gates is found in (B) and (C) as shown in Figure 9 is 60 fs, other outputs are respectively 110 and 100 fs in outputs (A) and (D). The latency of our gates was calculated as per[26].

5. Conclusion

In this study, we presented a novel design for all-optical logic gates, include all-optical logic gates, based on a 2D simulation utilizing Finite-Difference Time-Domain (FDTD) and Plane Wave Expansion (PWE) techniques. The proposed design involved removing elliptical Si-rods from the Si substrate and replacing them with air-holes to enable light manipulation through air waveguides. The significant advantage of this design is the compact size of the gates and low response time, meeting the requirements for downscaled all-optical devices, as well as the ease of fabrication and the novelty of the TM-only polarization. We compare our design with previous and recent work in Table 5, showing that while both TM and TE polarizations have been implemented before, they required complex and challenging techniques. In contrast, our design is simpler to fabricate and utilizes more accessible materials, making it a promising candidate for practical applications in all-optical computing.

Table 8 (comparison of proposed results with previously published results)

Ref(year)	gates	Polarization	Technique	Dimensions(μm^2)	CR (db)	Response time (fs)
This paper	All gates	TM	Interference effect	4*4	4~7.4	60~110
[27] (2016)	All gates	Polarization independent	Non liner kerr material	____	6-10	310~360
[28] (2016)	XOR and OR	TE	Interference effect	11.6*11.6	6.767	400
[29](2019)	NOT and AND	____	MOPSO-based inverse-design	1.2*1.2	3.9~7.1	250
[30](2020)	OR, AND, NOR and NAND	TE	Line defect and square resonator	13.34*13.34	2.9~6.1	250~1100
[26](2020)	XOR and OR	TE	Interference effect	12.5*12.5	____	90~120
[31] (2021)	AND	TE	Interference effect	7*7	____	60

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